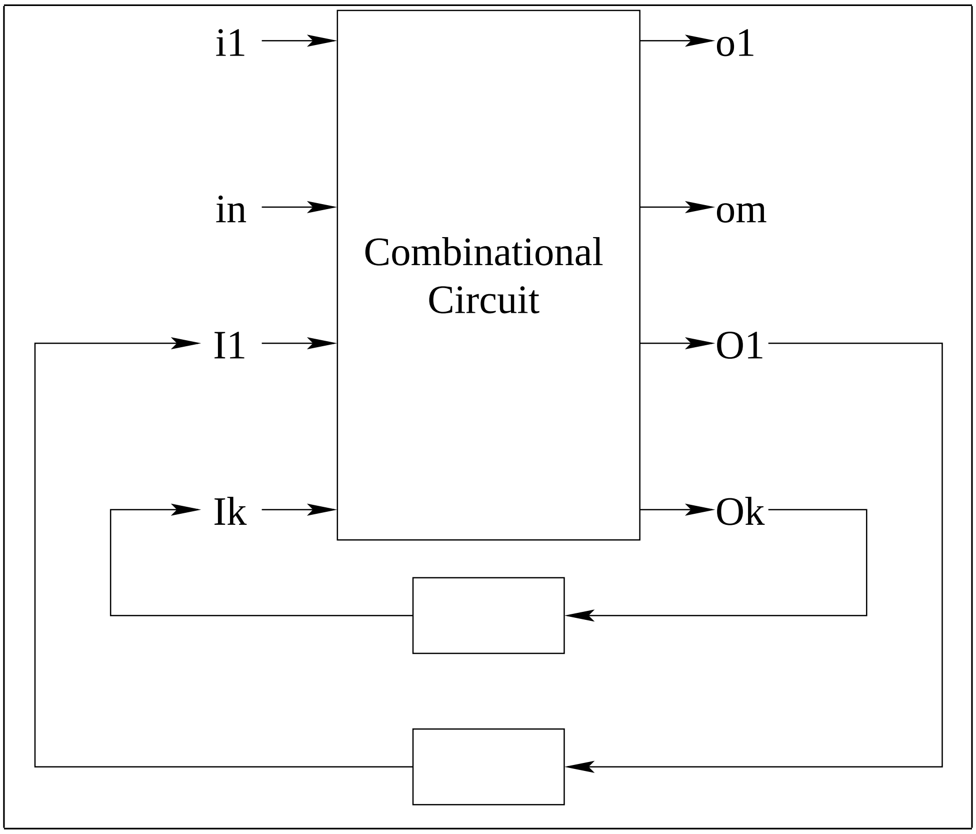
SEQUENTIAL CIRCUITS I



State of circuit = content of k memory cells.
One bit (0 or 1) per cell $\rightarrow 2^k$ possible states

Actual state is $I_1, \ldots, I_k$

Next state is $O_1, \ldots, O_k$

$$o_i = f(i_1, \ldots, i_n, I_1, \ldots, I_k),\ 1 \leq i \leq m$$
$$O_j = f(i_1, \ldots, i_n, I_1, \ldots, I_k),\ 1 \leq j \leq k$$

A sequential circuit is in a stable state when $I_j = O_j$ for $j = 1, \ldots, k$

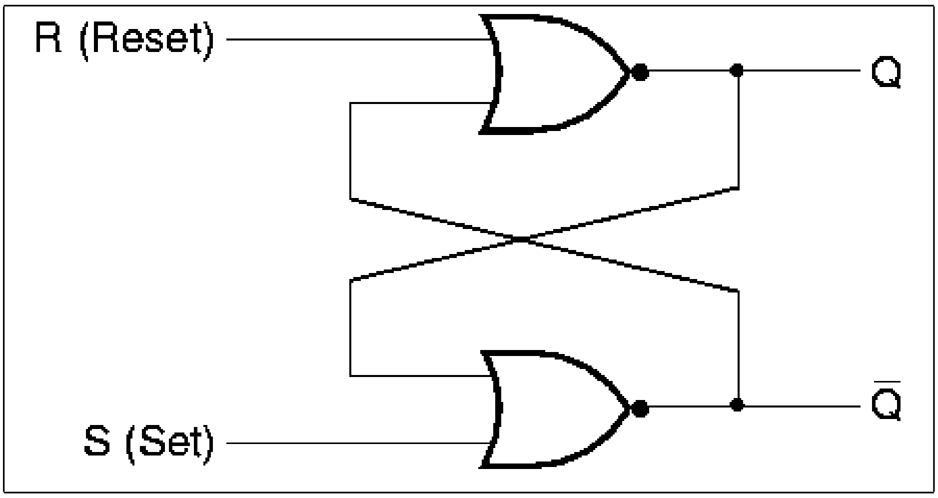
Asynchronous Sequential Circuits

Responds to a change in one of the inputs

Input signals change one at a time and only when the circuit is in a stable state

Memory elements = Latches: Two-state circuit that stores one bit

SR **latch:** 2 inputs (S)et, (R)eset, and 2 outputs $Q, \bar{Q}$



Its equations are:

$$Q = \overline{R + p} = \bar{R}\bar{p}$$

$$P = \overline{S + q} = \bar{S}\bar{q}$$

where p, q are the actual states and Q, P are the next states (with $P = \bar{Q}$)

Stable States of SR Latch

To find the stable states

- Obtain *truth table* of SR latch according to $Q = f(q, p, R, S) = \bar{R}\bar{p}$
  $P = f(q, p, R, S) = \bar{S}\bar{q}$
- Build a K-map with values of Q,P as entries
- Circle entries where Q,$P = q$,p

q	p	R	S	Q	P
0	0	0	0	1	1
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	0	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0

$\mapsto$

	00	01	11	10
00	11	10	00	01
01	01	00	00	01
11	00	00	00	00
10	10	10	00	00

Functionality of SR Latch (continued)

$S,R = 1,1 \mapsto$ stable state $Q,\bar{Q} = 0,0 \rightarrow Q = \bar{Q}$ $\rightarrow$ undefined state. We must avoid inputs $S,R = 1,1$ simultaneously

$Q,\bar{Q} = 0,0 \mapsto$ indeterminate next state when S,R becomes 0,0 simultaneously.

	00	01	11	10
00	11	10	00	01
01	01	00	00	01
11	00	00	00	00
10	10	10	00	00

$S,R = 1,0 \mapsto$ set state $Q,\bar{Q} = 1,0$

$S,R = 0,1 \mapsto$ reset state $Q,\bar{Q} = 0,1$

$S,R = 0,0 \mapsto$ next state = actual state of $Q,\bar{Q}$

Functionality of SR Latch (continued)

S,R = 0,0

	00	01	11	10
00	11	10	00	01
01	01	00	00	01
11	00	00	00	00
10	10	10	00	00

S,R = 0,1

	00	01	11	10
00	11	10	00	01
01	01	00	00	01
11	00	00	00	00
10	10	10	00	00

S,R = 1,0

	00	01	11	10
00	11	10	00	01
01	01	00	00	01
11	00	00	00	00
10	10	10	00	00

S,R = 1,1

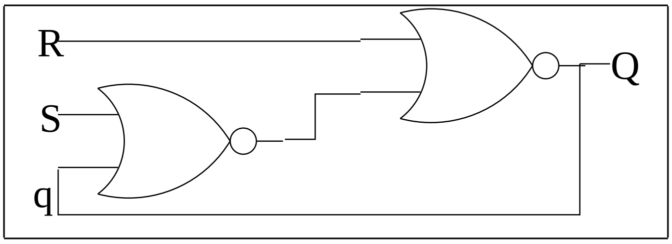
	00	01	11	10
00	11	10	00	01
01	01	00	00	01
11	00	00	00	00
10	10	10	00	00

Therefore the truth table of SR latch is

S	R	Q	$\overline{Q}$	
1	0	1	0	Set state
0	0	1	0	
0	1	0	1	Reset state
0	0	0	1	
1	1	0	0	Undefined

SR **Latch**

(equivalent representation)



Its equation is $Q = S\bar{R} + q\bar{R}$

Truth table and transition table below

q	R	S	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

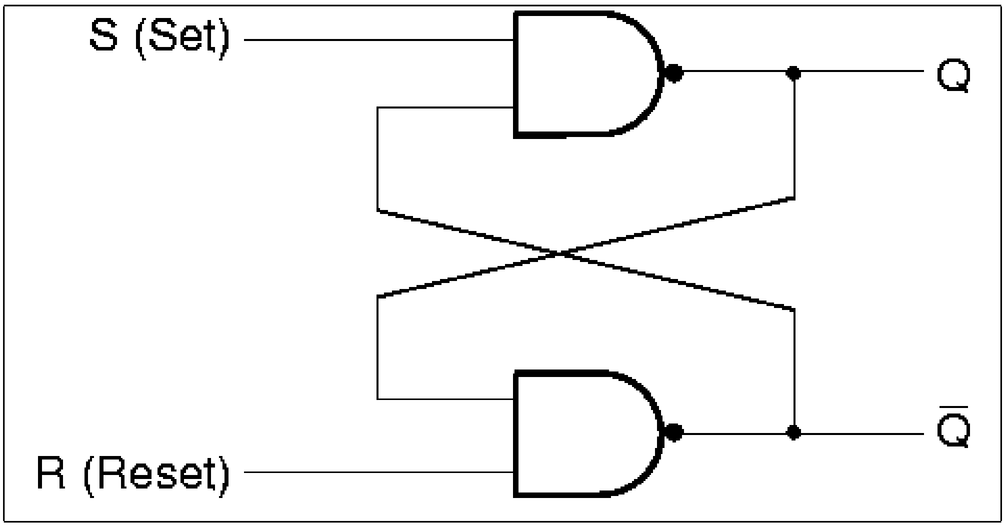
$\mapsto$

	00	01	11	10
0	0	1	X	0
0	1	1	X	0

$\Rightarrow$ if $SR = 0$ (S,$R \neq$ 1,1) then
minimal $\rightarrow Q = S + \bar{R}q$

$\bar{S}\bar{R}$ Latch

Uses NAND gates



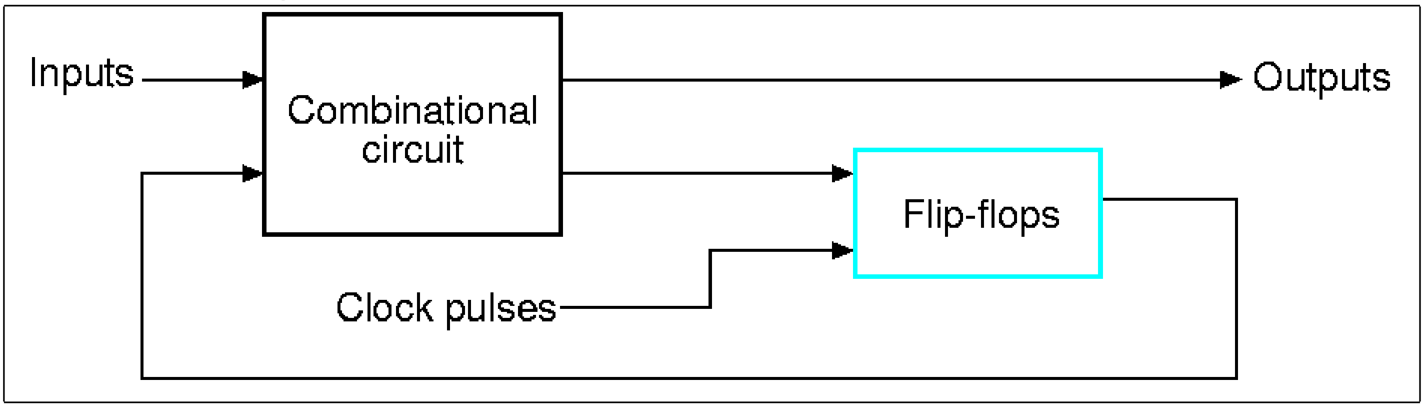
$\Downarrow$

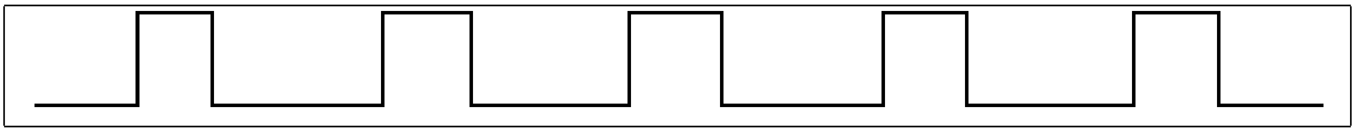
S	R	Q	$\bar{Q}$	
0	1	1	0	Set state
1	1	1	0	
1	0	0	1	Reset state
1	1	0	1	
0	0	1	1	Undefined

When $\bar{S}\bar{R} = 0$, that is S,$R \neq$ 0,0 then its equation is

$$Q = \bar{S} + Rq$$

Synchronous Sequential Circuits





Responds to a clock pulse

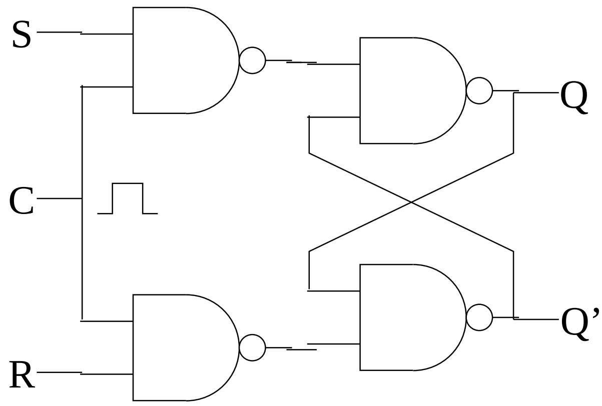
State transitions occurs only at fixed time intervals dictated by the clock pulses.

Time is discrete: the next state can be described at time $t+1$ with respect to the actual state at time t

More complex design but more reliable than asynchronous circuits.

Memory elements = Flip-flops: Two-state circuit that stores one bit

SR Flip-Flop



$\longrightarrow$

Q_t	S	R	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	?
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	?

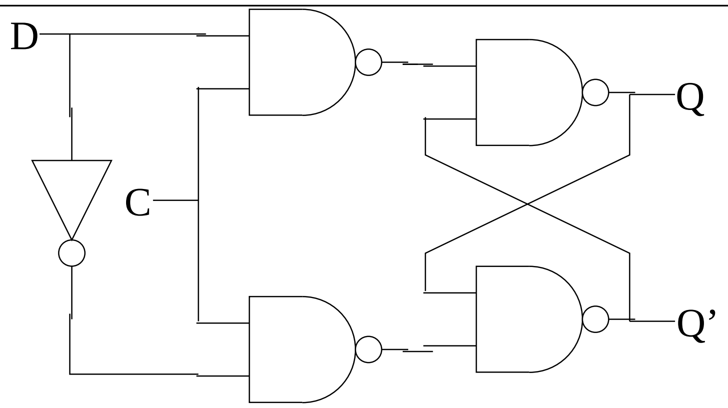
Working conditions: $SR = 0$. Pulse triggered flip-flop

Characteristic equation: (after simplification)

$$Q_{t+1} = S + \bar{R}Q_t$$

Characteristic table				**Excitation table**			
S	R	Q_{t+1}	Operation	Q_t	Q_{t+1}	S	R
0	0	Q_t	No change	0	0	0	X
0	1	0	Reset	0	1	1	0
1	0	1	Set	1	0	0	1
1	1	?	Undefined	1	1	X	0

D Flip-Flop



$\longrightarrow$

Q_t	D	Q_{t+1}
0	0	0
0	1	1
1	0	0
1	1	1

Working conditions: No undefined state. Edge triggered flip-flop

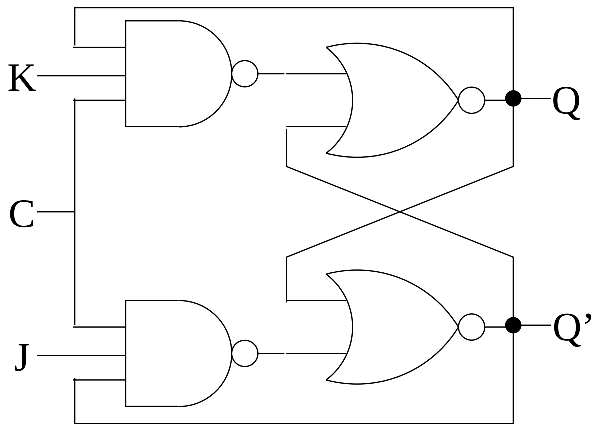
Characteristic equation: (after simplification)

$$Q_{t+1} = D$$

Characteristic table		
D	Q_{t+1}	Operation
0	0	Reset
1	1	Set

Excitation table		
Q_t	Q_{t+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

JK Flip-Flop



$\longrightarrow$

Q_t	J	K	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

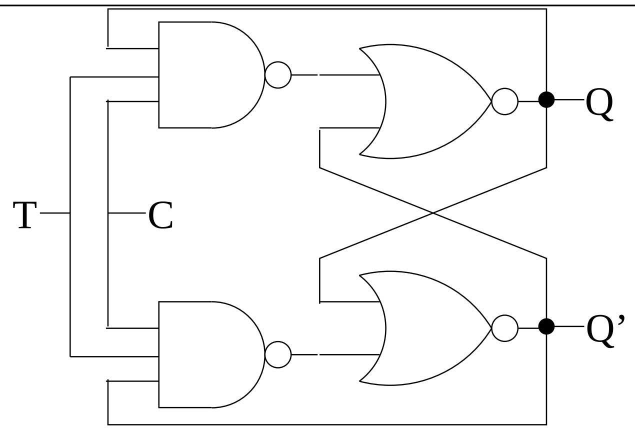
Working conditions: No undefined state. Pulse or edge triggered flip-flop

Characteristic equation: (after simplification)

$$Q_{t+1} = J\bar{Q} + \bar{K}Q$$

Characteristic table				Excitation table			
J	K	Q_{t+1}	Operation	Q_t	Q_{t+1}	J	K
0	0	Q_t	No change	0	0	0	X
0	1	0	Reset	0	1	1	X
1	0	1	Set	1	0	X	1
1	1	$\bar{Q}_t$	Complement	1	1	X	0

T Flip-Flop



→

Q_t	T	Q_{t+1}
0	0	0
0	1	1
1	0	1
1	1	0

Working conditions: No undefined state. Pulse or edge triggered flip-flop

Characteristic equation: (after simplification)

$$Q_{t+1} = T\bar{Q} + \bar{T}Q$$

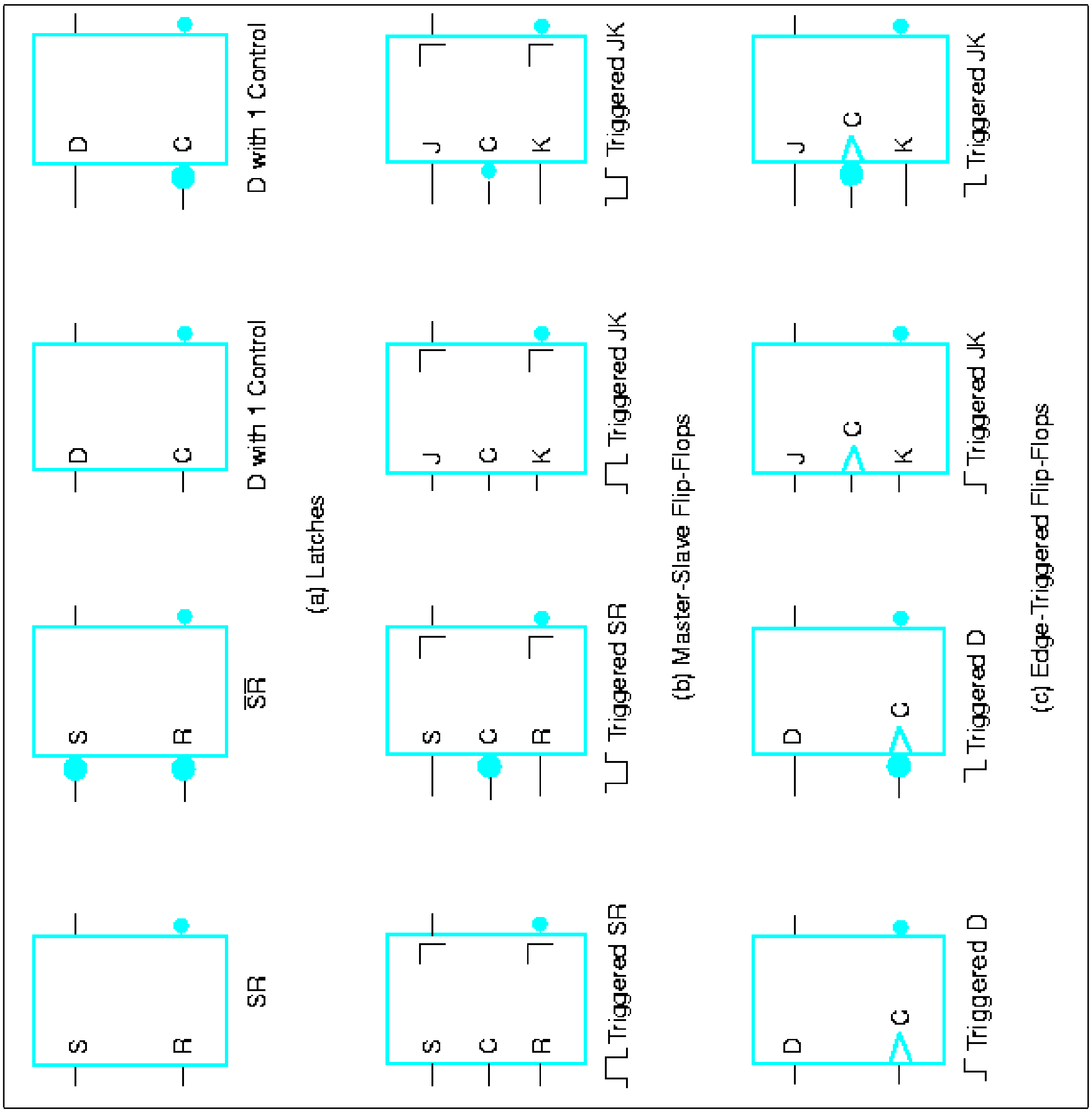
Characteristic table

T	Q_{t+1}	Operation
0	Q_t	Reset
1	$\bar{Q}_t$	Set

Excitation table

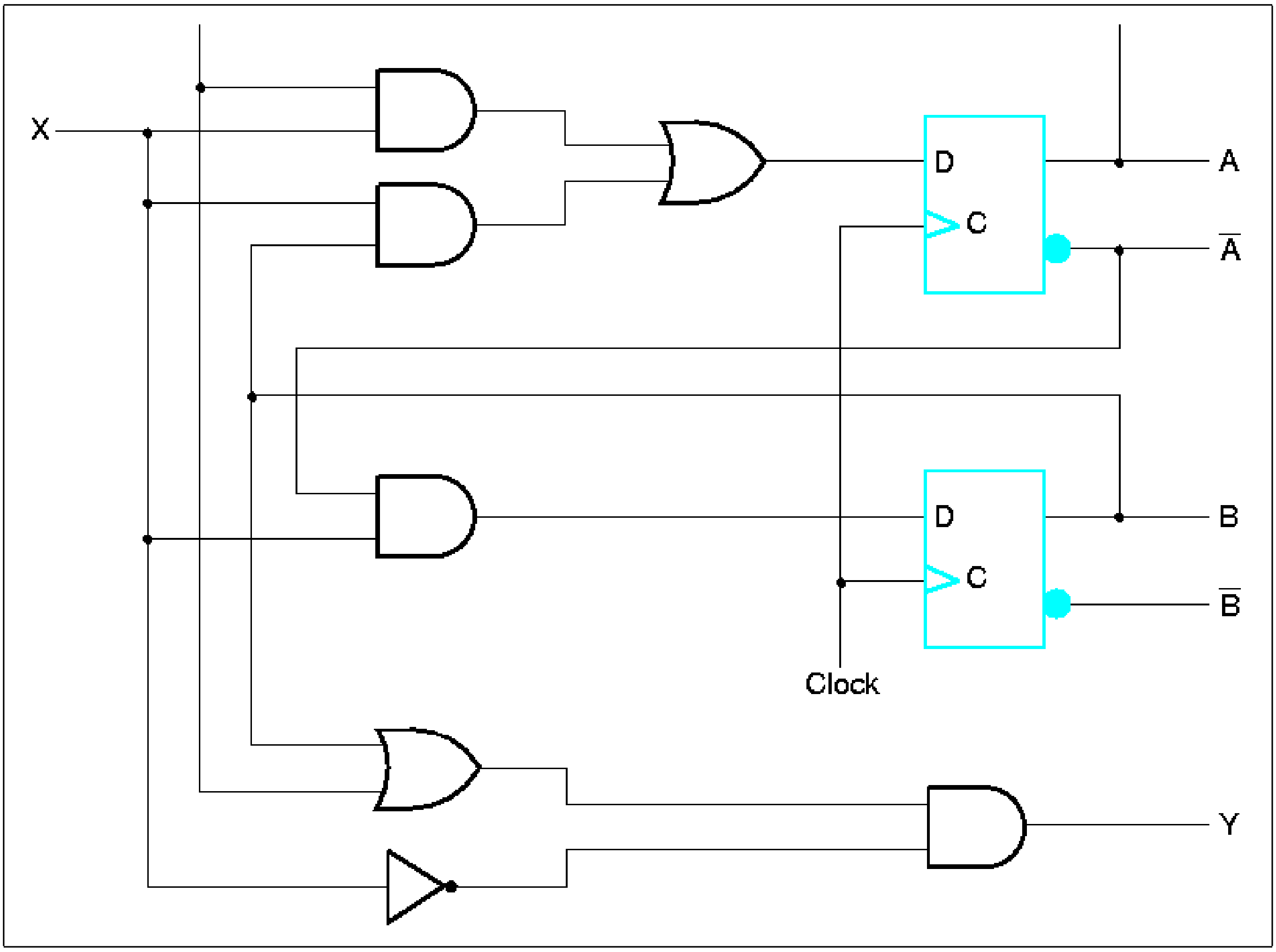
Q_t	Q_{t+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Standard Graphics Symbols for Latches and Flip-Flops



Synchronous Sequential Circuit Analysis

Given a synchronous sequential circuit, example



We can express its behavior in three ways: by

1. Circuit output functions and flip-flops input functions

2. Circuit output functions and state equations

3. State table and state diagram

Synchronous Sequential Circuit Analysis
(Circuit output and flip-flops input functions)

Question: What are the values of Y, D_A and D_B ?

Use the information contained in the combinational circuit to obtain the circuit's outputs and the flip-flops' inputs. That is

- $Y = \bar{X}(A_t + B_t)$
- $D_A = X(A_t + B_t)$
- $D_B = X\bar{A}_t$

Thus we can represent the states changes and the outputs. **However**, this representation is quite useless; we still do not know what the circuit truly does (particularly when we do not know the types of flip-flops used). The following two representations are better.

Synchronous Sequential Circuit Analysis

(Circuit output functions and state equations)

Question: Values of Y, A_{t+1} and B_{t+1} ?

For circuit's output functions: use the information contained in the combinational circuit. That is

- $Y = \bar{X}(A_t + B_t)$

For flip-flops' state equations: either

- Make a truth table and minimize to obtain the state equations. Or,
- Substitute the flip-flops' input functions into the flip-flops' characteristic equations to obtain the state equations

The characteristic equation of D flip-flop is $Q_{t+1} = D$, therefore

- $A_{t+1} = D_A = X(A_t + B_t)$
- $B_{t+1} = D_B = X\bar{A}_t$

Synchronous Sequential Circuit Analysis
(State table and state diagram)

Question: What are the ouputs and next states given the inputs and current states?

State table: Enumerates the functional relationships between inputs, outputs, and states flip-flops states of a sequential circuit

State diagram: Graphical representation of a state table

For each possible (actual) state of the circuit and for each possible combination of values of input variables:

1. Use the flip-flops' input functions and their characteristic tables to determine the next state of the circuit (A,B in example)

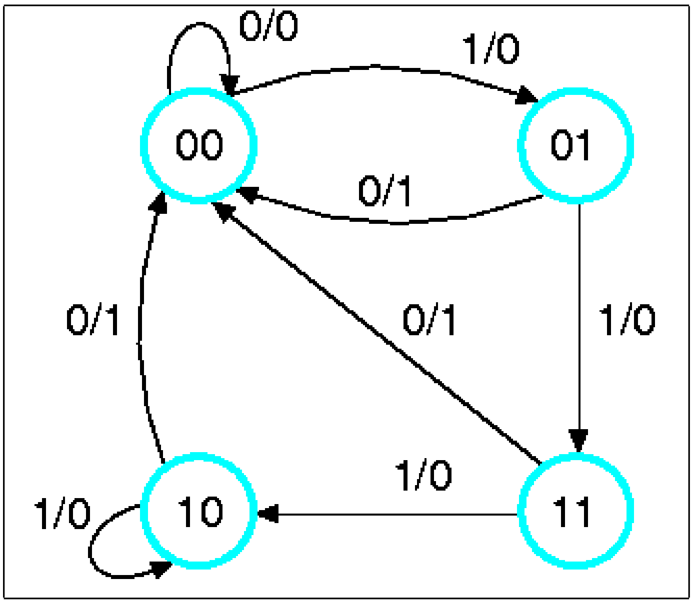
2. Use the circuit's output functions to determine the output values (Y in example)

Synchronous Sequential Circuit Analysis
(State table and state diagram)
(continued)

State Table

Present state		Next state				Output	
		$X=0$		$X=1$		$X=0$	$X=1$
A	B	A	B	A	B	Y	Y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

State Diagram



Synchronous Sequential Circuit Design

1. Obtain state table from circuit specification (state diagram, state equations or timing diagram)

2. If necessary, assign binary codes to each state of state table

3. Determine the number and type of flip-flops needed and assign a letter to each

4. From the state table, derive the circuit excitation and output tables

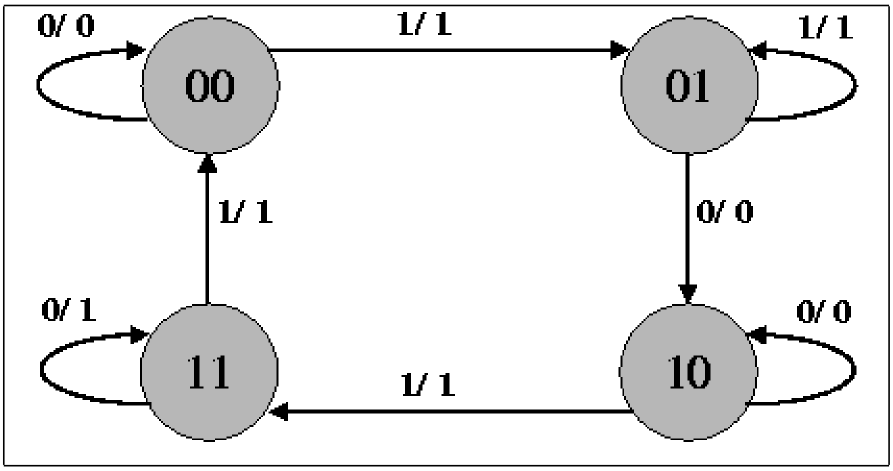
5. Using K-maps, derive the circuit output functions and the flip-flops input functions

6. Draw the synchronous sequential logic circuit

Synchronous Sequential Circuit Design
(Example)

Given the

State diagram



or the

State equations

$$
\begin{aligned}
Y &= A_t B_t + X \\
A_{t+1} &= A_t \bar{B}_t + B_t \bar{X} \\
B_{t+1} &= A_t B_t \bar{X} + \bar{A}_t x + \bar{B}_t X
\end{aligned}
$$

of a synchronous sequential circuit specification

Then . . .

. . . use the following design method . . .

Synchronous Sequential Circuit Design
(continued)

Step 1:

Present state		Next state				Output	
		$X=0$		$X=1$		$X=0$	$X=1$
A	B	A	B	A	B	Y	Y
0	0	0	0	0	1	0	0
0	1	1	0	0	1	0	1
1	0	1	0	1	1	0	1
1	1	1	1	0	0	1	1

Step 2: Not necessary in our example

Step 3:

Type of flip-flop is usually given. If not, then select cheapest: in general JK flip-flop

Number of flip-flops depends on number of states and the encoding used. In our case we need 2 flip-flops since there are 4 states ($2 = \log_2 4$), each coded by two variables. The flip-flops are:

$J_A K_A$ flip-flop and $J_B K_B$ flip-flop and

Synchronous Sequential Circuit Design (continued)

Step 4: Reorganize the state table in the following way

Inputs of CC				Inputs of FF			
Ps	Input	Ns	Output	Excitations			
AB	X	AB	Y	J_A	K_A	J_B	K_B
00	0	00	0	0	X	0	X
00	1	01	1	0	X	1	X
01	0	10	0	1	X	X	1
01	1	01	1	0	X	X	0
10	0	10	0	X	0	0	X
10	1	11	1	X	0	1	X
11	0	11	1	X	0	X	0
11	1	00	1	X	1	X	1

$\Uparrow$

Excitation table			
Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation table: what are the values of J and K needed to go from Q_t to Q_{t+1}?

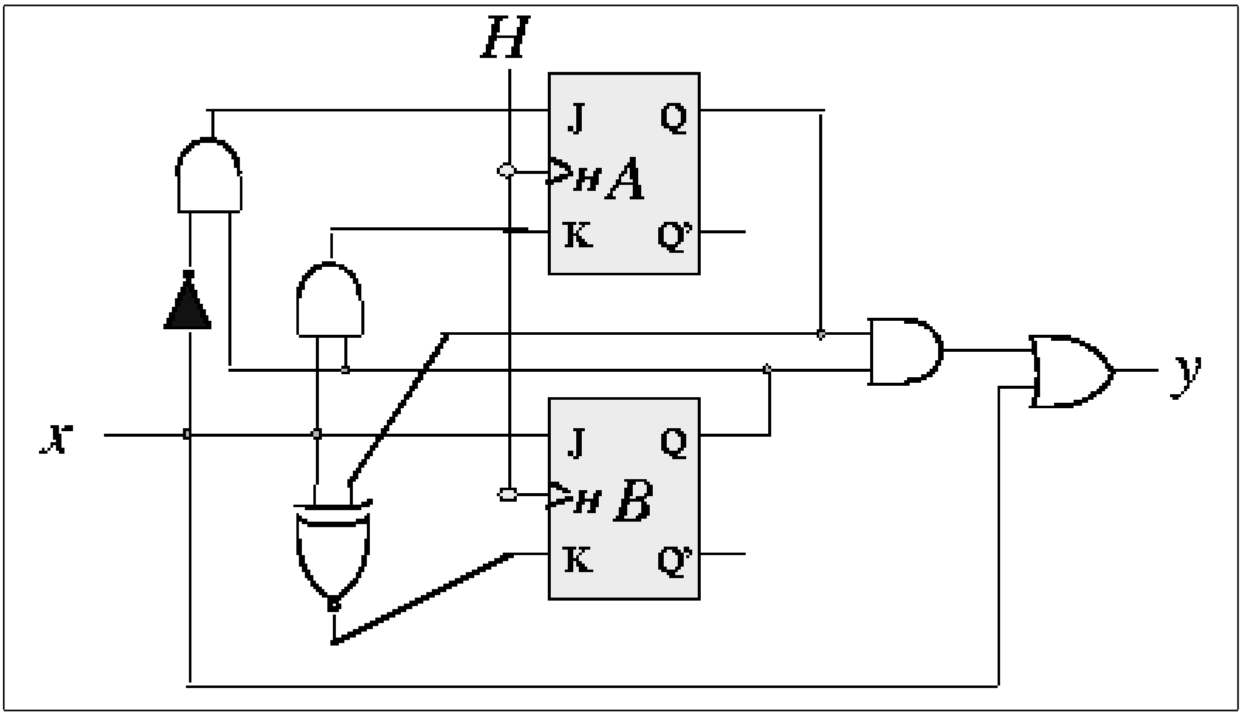
Synchronous Sequential Circuit Design
(continued)

Step 5: Simplify the by K-maps the circuit's output Y, and the flip-flops' inputs J_A, K_A, J_B and K_B. After simplification, we obtain:

- $Y = AB + X$
- $J_A = B\bar{X}$
- $K_A = BX$
- $J_B = X$
- $K_B = \bar{A}\bar{X} + AX = A \odot X$

Synchronous Sequential Circuit Design
(continued)

Step 6:



Use the standard graphics symbols for flip-flops

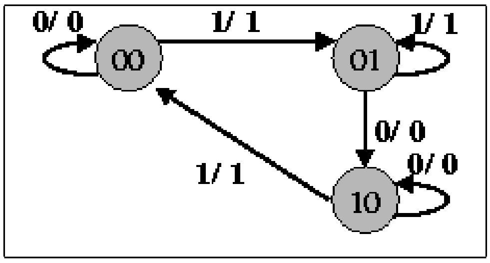
Clearly identify the inputs and outputs of the flip-flops, the clock input, as well as the external inputs and outputs of the circuit

Try to minimize crossings (difficult problem)

Clearly show the intersections

Synchronous Sequential Circuit Design
(continued)

Designing With Unused States: If a state is not used (state 11 below), then put an X for the flip-flops' inputs and the circuit's output. The final expressions will be much simpler



The table below shows only the part of the excitation table (obtained in step 4) that deals with the state 11

Inputs of CC				Inputs of FF			
Ps	Input	Ns	Output	Excitations			
AB	X	AB	Y	J_A	K_A	J_B	K_B
00	0						
00	1						
01	0						
01	1						
10	0						
10	1						
11	0	XX	X	X	X	X	X
11	1	XX	X	X	X	X	X